

2814  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: C. C. Cheng, et al.

Attorney Docket No.: 01-695/LSI1P184

Application No.: 09/996,118

Examiner: Rao, S. H.

Filed: 27 November 2001

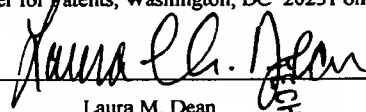
Group: 2814

Title: Low Resistance Metal Interconnect Lines  
And A Process For Fabricating Them

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Commissioner for Patents, Washington, DC 20231 on May 23, 2002.

Signed:

  
Laura M. Dean

**AMENDMENT A TRANSMITTAL**

Commissioner for Patents  
Box Non-Fee Amendment  
Washington, DC 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

The fee has been calculated as shown below.

	Claims After Amendment		Highest Previously Paid For	Present Extra	Small Entity Rate Fee	Large Entity Rate Fee
Total Claims	5	MINUS	20	0	x 9 = 0	x 18 = 0
Independent Claims	1	MINUS	3	0	x 42 = 0	x 84 = 0
Multiple Dependent Claim Present and Fee Not Previously Paid					\$140.00	\$280.00
Total					\$	\$




Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 12-2252 (Order No. 01-695/LSI1P184).



Please charge the required fees, or any additional fees required to facilitate filing the enclosed response, to Deposit Account No. 12-2252 (Order No. 01-695/LSI1P184).

Respectfully submitted,  
BEYER WEAVER & THOMAS, LLP

  
Steve D Beyer  
Reg. No. 31,234

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Title: Low Resistance Metal Interconnect Lines  
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 Laura M. Dean
**AMENDMENT A**

Commissioner for Patents  
Box Non-Fee Amendment  
Washington, D.C. 20231

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Dear Sir:

In response to the Office Action dated 20 March 2002 please amend the above identified patent application as follows:

**In the Claims:**

All pending claims have been reproduced below for the convenience of the Examiner. Claims which have been changed by this amendment are indicated with "(Once Amended)".

Please **cancel** claims 1 through 5, without prejudice.

6. (Once Amended) A method for fabricating low resistance interconnect lines in an integrated circuit, the method comprising the steps of:

patterning and etching a dielectric layer in an integrated circuit;

filling the etched areas of the dielectric layer with copper;